# AN-CM2511

POWERMASTER SEMICONDUCTOR

Masters of Power Solution

# 1200V *e*SiC M2 MOSFET Series

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# 1. Introduction

The automotive industry is rapidly transitioning toward electrification due to rising demand for sustainable transportation, which has led to an increased need for high-performance power electronics in electric vehicle (EV) applications. The main drivers for adopting new technologies in EVs are the improvement of efficiency and power density in power electronic systems. The three-phase inverter topology dominates traction inverters and e-compressors used in electric vehicles due to their high efficiency and simple control requirements, as shown in Fig. 1. The 1200V silicon carbide (SiC) MOSFETs are gaining significantly popularity for traction inverters, and the e-compressors, which are indispensable power conversion systems that ensure efficient thermal management, extend battery life, improve charging efficiency, and driving range, and maintain a comfortable environment for electric vehicles [1]. SiC MOSFETs are also optimized for bridge topologies such as three phase B6 and CLLC/DAB (Dual Active Bridge) topologies due to , which are essential for bidirectional power conversion, a key trend in onboard chargers (OBC) for 800V battery system in EVs. These devices provide system level benefits, including lower power losses, reduced system volume, weight and cost advantages for high voltage battery-powered systems. For motor drive applications, short-circuit robustness is a key requirement for power semiconductor devices. Silicon IGBTs are still preferred due to their cost-effectiveness, reasonable efficiency, and good short-circuit capability (approximately 10 μs). However, recent advancements in SiC MOSFET technology have enabled improved efficiency and power density, as these devices exhibit superior thermal performance, higher switching frequencies, higher power density, and lower on-resistance and switching losses compared with Si IGBTs. Despite these advantages, SiC MOSFETs have a significant drawback that is limited short-circuit capability. This limitation arises from the higher electric field at the P-N junction, lower heat capacity and smaller die size compared to Si IGBT with same voltage and current ratings. The inferior short-circuit capability of SiC MOSFETs can lead to catastrophic failures such as gate oxide failure or thermal runaway during short-circuit events [2]-[3]. Therefore, short-circuit protection (SCP) is crucial to prevent device failure. The protection circuit must respond within few microseconds under fault conditions to ensure safe and reliable operation, particularly short-circuit (SC) events. To enhance short-circuit ruggedness, many studies have proposed such as reducing channel/JFET density, lowering source doping, or using lower gate bias [4]-[6]. However, these approaches typically increase the specific on-resistance ($R_{sp}$).

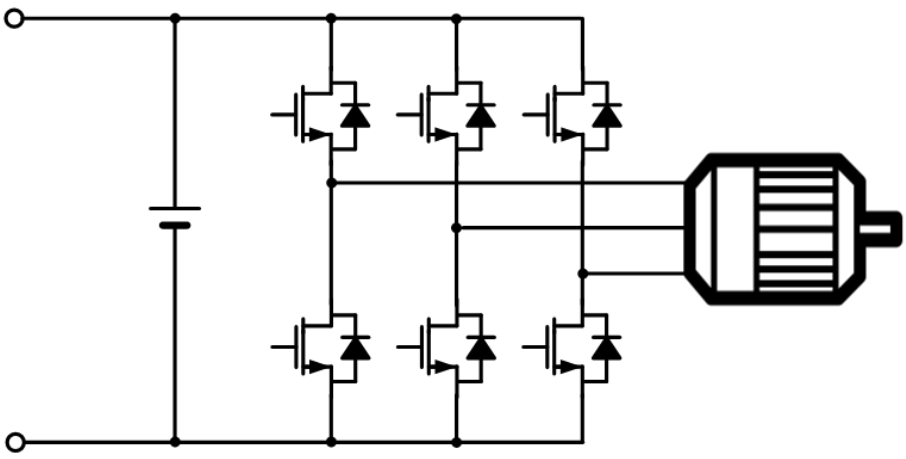


**Figure 1.** Diagram of three phase inverter

This application note presents a new generation of 1200V silicon carbide (SiC) MOSFETs (*e*SiC, M2), which employ a novel device technology that significantly mitigates the trade-off between the figure of merits (FOMs) and short-circuit withstand time (SCWT). Compared to the previous generation, the new 1200V *e*SiC M2 MOSFET series exhibits a 20% reduction in on-resistance ($R_{sp}$), a 15% improvement in SCWT, and a 45% reduction in switching losses. Furthermore, it provides a comparison of key characteristics, including short-circuit ruggedness and switching performance, with planar and trench 1200V SiC MOSFETs.

# 2. 1200V *e*SiC M2 MOSFET Technology

For SiC MOSFETs, the channel resistance contributes significantly to the total on-resistance ($R_{DS(ON)}$) due to the low channel mobility compared to that of Si MOSFETs. One effective way to reduce channel resistance is to decrease the cell pitch. However, when the cell pitch is reduced, the JFET width must also decrease inevitably, which increases the JFET resistance by narrowing the current path within the JFET region. To mitigate this, additional heavy doping in the narrow JFET region can be applied to lower the JFET resistance. The new 1200V *e*SiC M2 MOSFET features a novel device structure that simultaneously reduces key figures of merit (FOMs) and enhances short-circuit withstand time - two characteristics that are typically in trade-off with each other. This improvement is achieved by reducing the cell pitch and narrowing the JFET width, thereby optimizing specific on-resistance ($R_{sp}$) and short-circuit ruggedness.

## 2.1. Improved Turn-on/Turn-off Switching Loss by Low Gate-Drain Capacitance

Gate-to-drain capacitance, $C_{GD}$ ($C_{rss}$), also known as feedback or the reverse transfer capacitance, plays a crucial role in switching performance. When $C_{rss}$ is large, the drain current takes longer to rise even after the gate is turned on, and the falling current is similarly delayed when the gate is turned off. This parameter greatly affects the switching speed. As shown in Fig. 2, $C_{rss}$ is proportional to the width of the JFET region. By narrowing the JFET width, $C_{rss}$ of the new 1200V *e*SiC M2 MOSFET under high voltage conditions was significantly reduced (M1: 9pF, M2: 4pF at $V_{DS}$ = 800V) compared to the with previous generation 1200V *e*SiC M1 MOSFET as shown in Fig. 3. Fig. 4 shows the total gate charge measurement of the new 1200V, 40mΩ *e*SiC M2 MOSFET and the previous generation under the same conditions ($V_{DS}$=800V, $V_{GS}$=-3~10V, and $I_D$=30A). The total gate charge ($Q_G$) and gate-drain charge ($Q_{GD}$) of new 1200V, 40mΩ *e*SiC M2 MOSFET are reduced by 40% compared to those of the previous generation.

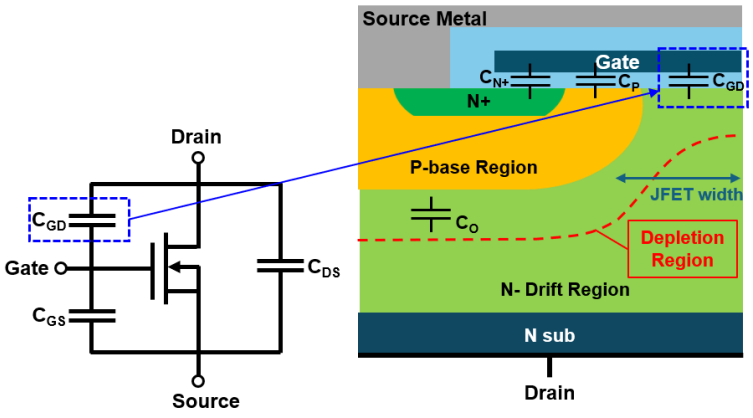



**Figure 2.** Capacitances for the vertical power MOSFET structure

In hard−switching applications, the MOSFET channel conducts a higher current than load current during turn−on, because of the additional discharging current from the output capacitance. Therefore, $E_{OSS}$ of the MOSFET during turn-off is internally dissipated through the MOSFET channel during turn−on. The stored energy in output capacitance, $E_{OSS}$ of the MOSFET, is especially critical in hard−switching applications, such as power factor correction (PFC), particularly at light loads, because it is fixed and independent of the load current. The reduction in $Q_{OSS}$ is critical for achieving zero-voltage switching (ZVS), the dead time between the high side and low side MOSFETs in the same leg must be long enough to allow the voltage transition. The new 1200V, 40mΩ *e*SiC M2 MOSFET has approximately 33% less stored energy in the output capacitance ($E_{OSS}$) and charge on the output capacitance ($Q_{OSS}$) than those of the previous generation under same conditions as shown in Fig. 5.

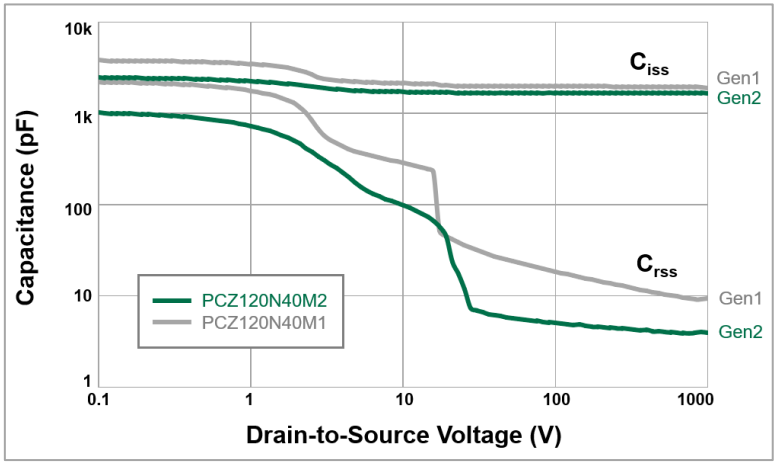



**Figure 3.** Comparison of capacitance characteristics ($C_{iss}$ and $C_{rss}$) of the new 1200V *e*SiC MOSFET M2 and previous generation (M1).

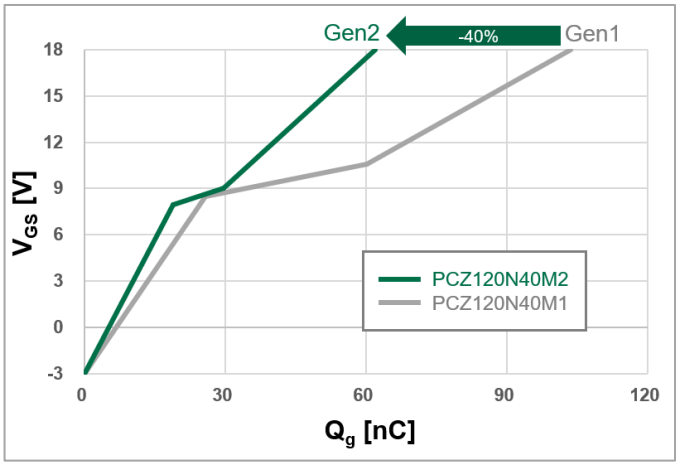



**Figure 4.** Comparison of gate charge ($Q_G$) of the new 1200V *e*SiC M2 MOSFET and previous generation.

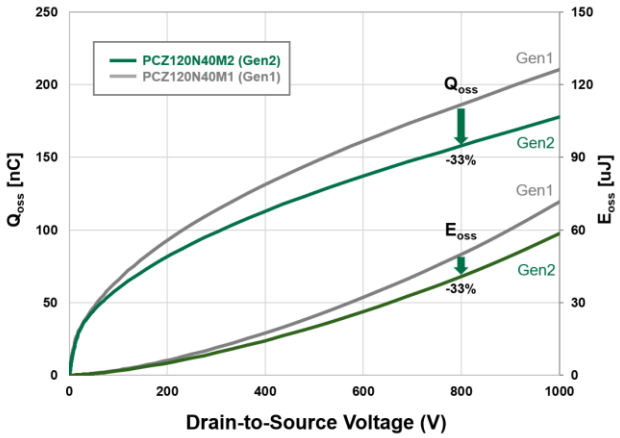
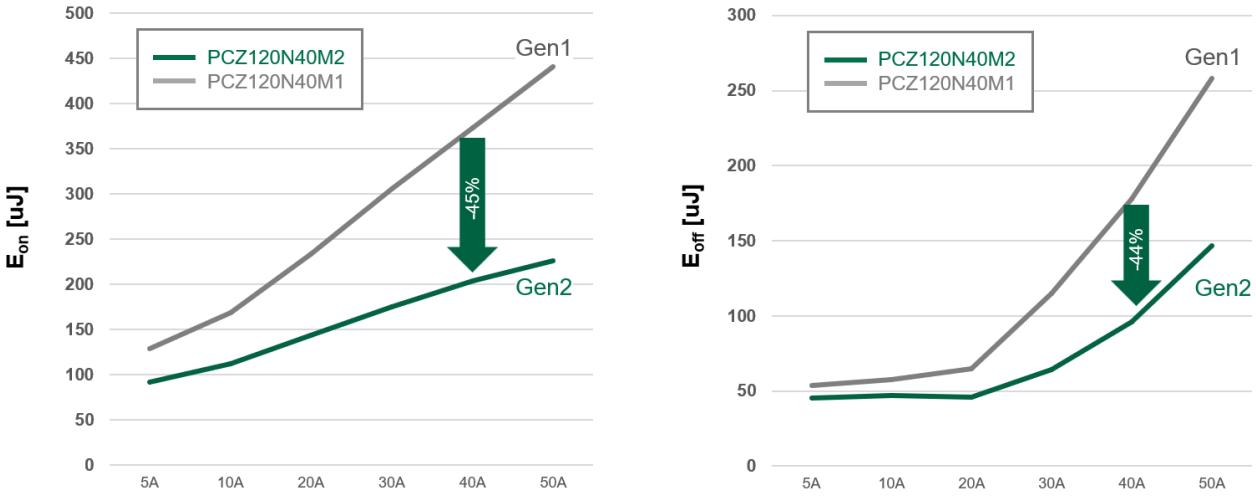



**Figure 5.** Comparison of $E_{OSS}$ and $Q_{OSS}$

The new 1200V *e*SiC M2 MOSFET has improved key figures of merit (FOMs) such as $R_{DS(ON)}{\cdot}Q_G$, $R_{DS(ON)}{\cdot}E_{OSS}$ and $R_{DS(ON)}{\cdot}Q_{OSS}$ by 33% to 40% compared to the previous generation. It also offers excellent switching performance, achieving 44% lower switching losses compared to the previous generation through significantly lower gate charge ($Q_G$) and reverse transfer capacitance ($C_{GD}$) as shown in Fig. 6

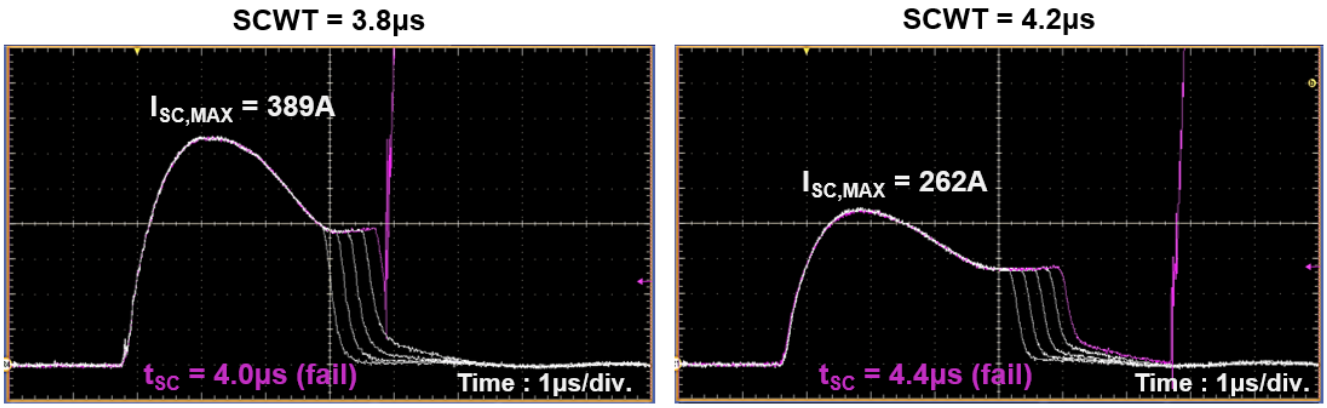



(a) $E_{on}$ (b) $E_{off}$

**Figure 6.** Comparison of switching losses of the new 1200V *e*SiC M2 MOSFETs vs. previous generation under $V_{DD}$=800V, $V_{GS}$=-3V/+18V, $R_G$=4.7Ω, Free-wheeling Diode: Same DUT

## 2.2. Short-Circuit Withstand Time (SCWT) Capability

To effectively reduce the peak current in SiC MOSFETs during short-circuit conditions, it is crucial to enhance the JFET effect within the p-body regions. A narrower JFET region helps to limit the saturation current at high drain voltage bias and improves the short circuit capability. The saturation current is predominantly influenced by the channel design. Although reducing the channel length and increasing gate driving voltage can reduce on-resistance, they also increase the saturation current, resulting in a reduced short circuit withstand time (SCWT). In the new 1200V *e*SiC M2 MOSFET structure, the short circuit current is limited by the narrow JFET region under high-voltage short-circuit conditions. This new design enables improved SCWT performance. Fig. 7 presents the short-circuit waveforms of the previous generation and the new 1200V *e*SiC M2 MOSFET under $V_{GS}$=15V, $V_{DD}$=800V and $R_G$=50Ω. The peak drain current in the new 1200V *e*SiC M2 MOSFET (262A) is reduced by 33% compared to that of the previous generation SiC MOSFET (389A), resulting in 11% improvement in short circuit withstand time (SCWT) due to the effect of its narrow JFET width. The trade-off between figure of merits (FOMs) is significantly improved by applying a channeling implantation technique. Consequently, the new 1200V *e*SiC M2 MOSFET not only improves on-resistance and switching performance, but also enhances short circuit robustness.




(a) Previous generation (b) New 1200V SiC MOSFET

**Figure 7.** Short-circuit waveforms comparison of previous generation and the new 1200V SiC MOSFETs

# 3. Performance Benchmark of 1200V *e*SiC M2 MOSFET

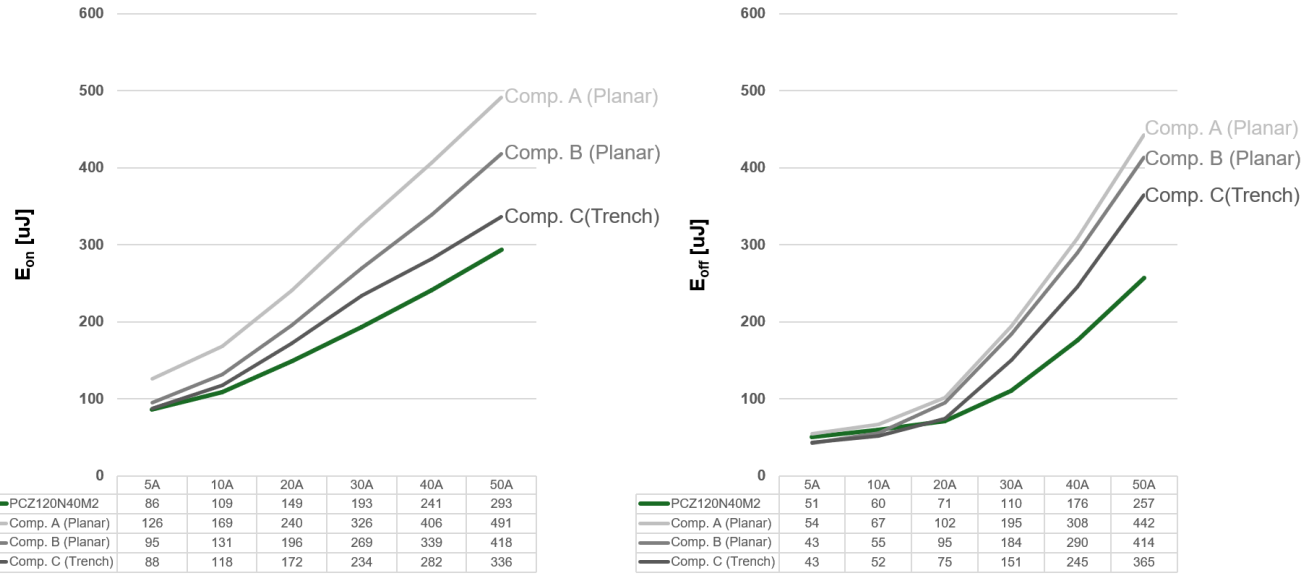
Table 1 presents a comparison of the key parameters for the new 1200V *e*SiC M2 MOSFETs. The 1200V *e*SiC M2 MOSFET (PCZ120N40M2) offers several advantages, including lower switching losses, extended short-circuit withstand time, and enhanced avalanche capability, all of which contribute to improved system efficiency and reliability.

| Specification | PCZ120N40M2 (Planar) | Comp. A (Planar) | Comp. B (Planar) | Comp. C (Trench) |
|---|---|---|---|---|
| **$BV_{DSS}$ [V]** | 1200 | 1200 | 1200 | 1200 |
| **$I_D$ [A]** | 57 | 66 | 54 | 55 |
| **$V_{GS\_op}$ [V]** | -3 / +18 | -4 / +15 | -3 / +18 | 0 / +18 |
| **$V_{GS\_max}$ [V]** | -10 / +22 | -8 / +19 | -10 / +22 | -10 / +23(pulse) |
| **$R_{DS(on)}$ [mΩ]** (typ) | 40 | 40 | 40 | 39 |
| **$V_{TH}$ [V]** | 2.0 / 3.0 / 4.5 | 1.8 / 2.7 / 3.6 | 2.0 / 2.9 / 4.4 | 3.5 / 4.2 / 5.2 |
| **$Q_G$ [nC]** | 62 | 94 | 66 | 50 |
| **$E_{ON}$ [μJ] @ $I_D$=40A, $R_G$=6.8Ω** | 241 | 406 | 339 | 282 |
| **$E_{OFF}$ [μJ] @ $I_D$=40A, $R_G$=6.8Ω** | 176 | 308 | 290 | 245 |
| **$E_{DYN}$ [uJ] @ $V_{DD}$=800V** | 5.3 | 7.5 | 5.3 | 6.0 |
| **$I_{AS}$ [A[ @ L=1mH, $R_G$=25Ω** | 41 | 46 | 34 | 40 |
| **SCWT [μs] @ $V_{DD}$=800V, $V_{GS}$=15V** | 4.2 | 2.2 | 2.6 | 5.0 |

**Table 1**. Key Parameter Comparison of Power Master Semiconductor's 1200V, 40mΩ *e*SiC M2 MOSFET (PCZ120N40M2) and Competitors

## 3.1. Switching Characteristics

Fig. 8 shows a comparison of the measured switching losses for the 1200V, 40mΩ *e*SiC M2 MOSFET (PCZ120N40M2) and competitor devices (planar and trench). The switching measurements were conducted with $V_{DD}$=800V, $V_{GS}$=-3V/+18V, $R_G$=6.8Ω, under various $I_D$ conditions. The experimental results show that turn-on loss ($E_{on}$) is reduced by 15% and 41%, while the turn-off loss ($E_{off}$) is reduced by 28 % and 43 % for the 1200V, 40mΩ *e*SiC M2 MOSFET (PCZ120N40M2) compared to that of competitor C (trench) and competitor A (planar), respectively, under the same conditions.




| | 5A | 10A | 20A | 30A | 40A | 50A |
|---|---|---|---|---|---|---|
| PCZ120N40M2 | 86 | 109 | 149 | 193 | 241 | 293 |
| Comp. A (Planar) | 126 | 169 | 240 | 326 | 406 | 491 |
| Comp. B (Planar) | 95 | 131 | 196 | 269 | 339 | 418 |
| Comp. C (Trench) | 88 | 118 | 172 | 234 | 282 | 336 |

| | 5A | 10A | 20A | 30A | 40A | 50A |
|---|---|---|---|---|---|---|
| PCZ120N40M2 | 51 | 60 | 71 | 110 | 176 | 257 |
| Comp. A (Planar) | 54 | 67 | 102 | 195 | 308 | 442 |
| Comp. B (Planar) | 43 | 55 | 95 | 184 | 290 | 414 |
| Comp. C (Trench) | 43 | 52 | 75 | 151 | 245 | 365 |

**Figure 8.** Comparison of switching losses - 1200V, 40mΩ $e$SiC M2 MOSFET vs. competitors under $V_{DD}$=800V, $V_{GS}$=-3V/+18V, $R_G$=6.8Ω, free-wheeling diode: Same DUT

## 3.2. Short-circuit capability (SCWT)

During the device operation, unexpected faults can occur in bridge type circuits, where failures often happen by short circuits in the high side and low side devices. In such cases, the device channel may accidentally conduct current while the device withstands the high drain-source voltage. This leads to high current density within the device, which can ultimately result in device failure. Short-circuit events can occur in a variety of ways in various motor drive systems used in both industrial and automotive applications. Approximately 38% of inverter failures are caused by power device failures due to short-circuit (SC) stresses. The short-circuit performance under the same conditions is determined by device design and manufacturing processes. 1200V, 40mΩ SiC MOSFETs listed in Table 1 were tested under short-circuit conditions to evaluate their short-circuit capability. A gate-source voltage is applied to the gate terminal of the device under test (DUT), and the short-circuit duration is controlled by adjusting the pulse width. The short-circuit duration gradually increases until the device reaches a failure point. The short-circuit waveforms, shown in Fig. 9, were measured under the following conditions: The gate-source voltage ($V_{GS}$) = 15V. bus voltage = 800 V, with the short-circuit time increased by 0.2μs steps until failure occurred. According to table 2, the maximum current of the new 1200V $e$SiC MOSFET M2 is 33% to 37% lower than those of competitor A and B, resulting in a reduction in junction temperature and a small positive feedback effect. The short-circuit withstand time (SCWT) for the new 1200V $e$SiC MOSFET M2, competitor A, B and C are 4.2μs, 2.4μs, 1.8μs and 4.6μs, respectively. The new 1200V $e$SiC MOSFET M2 demonstrates an improvement in short-circuit capability, being approximately 1.8~2.3 times better than those of competitor A and B, respectively, thanks to its novel design. The higher peak currents observed in competitor A and B lead to increased energy dissipation, resulting in a faster rise in junction temperature and a corresponding decrease in SCWT.

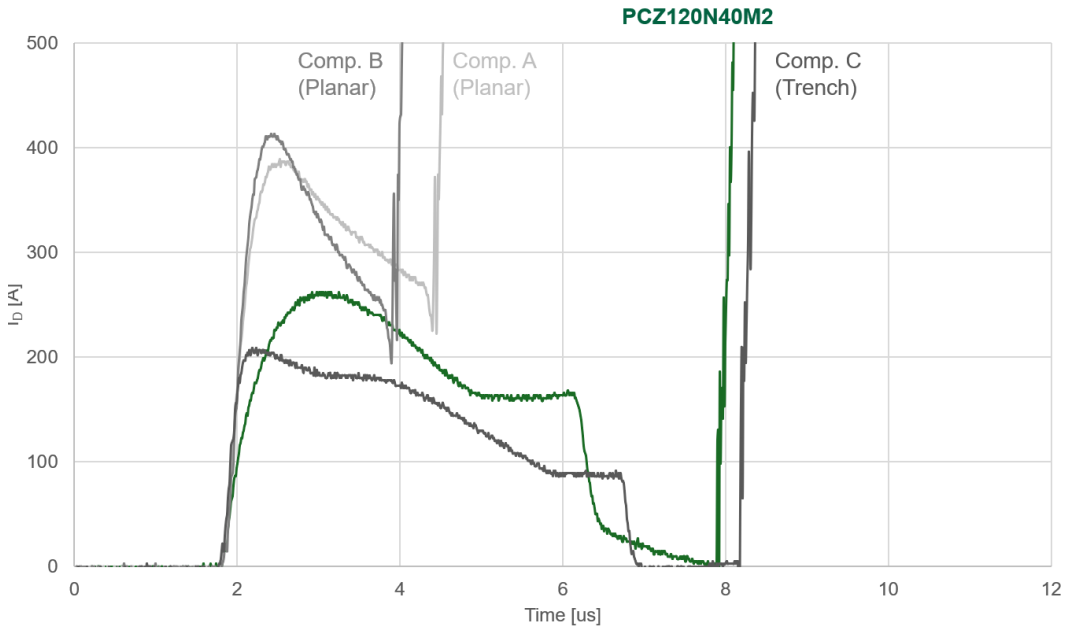



**Figure 9.** Comparison of short-circuit waveforms (SCWT) - 1200V, 40mΩ *e*SiC M2 MOSFET (PCZ120N40M2) vs. competitors under $V_{DD}$=800V, $V_{GS}$=-15V, $R_G$=50

| Package | DUTs | SCWT [µs] | $I_{SC}$ [A] |
|---|---|---|---|
| TO-247-4L | PCZ120N40M2 | 4.2 | 262 |
| | Comp. A (Planar) | 2.4 | 389 |
| | Comp. B (Planar) | 1.8 | 413 |
| | Comp. C (Trench) | 4.8 | 238 |

**Table 2.** Short-circuit current ($I_{SC}$) and withstand time (SCWT) comparison of Power Master Semiconductor's 1200V, 40mΩ *e*SiC M2 MOSFET (PCZ120N40M2) and Competitors.

## 4. Conclusion

The new 1200V *e*SiC M2 MOSFET technology achieved both lower figure of merits (FOMs) and improved short-circuit withstand time (SCWT) by employing a reduced cell pitch with a narrow JFET width, where the doping is uniformly applied across the entire JFET region. The new 1200V *e*SiC M2 MOSFET offers substantial system-level benefits, including smaller size, reduced weight, higher efficiency, lower cooling requirements, and enhanced reliability. These advantages stem from significantly lower power losses and improved short circuit ruggedness, making it ideal for a wide range of power conversion applications.

# 5. Reference

[1] Chaouite, Y. J., Islam, S. M., Al-Saffar, M. A., & Rahman, M. A. “SiC MOSFETs: The Inevi-table Trend for 800V Electric Vehicle Air Con-ditioning Compressors.” IEEE Transactions on Industry Applications, 61(3), 2345-2353. 2025

[2] Lee, S., & Cho, B. “Comparative study on short-circuit behaviour of SiC MOSFETs and Si IGBTs under inductive load conditions.” IEEE Transactions on Industrial Electronics, 65(9), 7321-7329.. 2018

[3] Park, J., & Lee, K. “Analysis of short-circuit withstand capability of SiC MOSFETs consid-ering thermal effects.” IEEE Transactions on Power Electronics, 34(3), 2345-2353. 2019

[4] Tanaka, H., & Saito, T. “Improved Short Cir-cuit Ruggedness by Optimization of Sidewall P-Type Pillar in Trench Gate SiC-MOSFET.” IEEE Transactions on Power Electronics, 38(9), 4567-4575. 2023

[5] Yamamoto, K., & Fujita, H. “Substantial Im-provement of the Short-Circuit Capability of a 1.2 kV SiC MOSFET Using a Composite Gate Stack.” IEEE Electron Device Letters, 45(2), 234-237. 2024

[6] Nakamura, Y., & Takeda, K. “Improved HF-FOM and SC Ruggedness of Split-Gate 4H-SiC MOSFETs”. IEEE Transactions on Elec-tron Devices, 71(1), 12-18. 2024

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# 6. 1200V $e$SiC MOSFET M2 Product Portfolio & Nomenclature

## 6.1. 1200V $e$SiC MOSFET M2 Product Portfolio

**Table 1.** 1200V $e$SiC MOSFET M2 Product Portfolio

| Package / $R_{DS(ON)\_typ}$ | Grade | Bare Die | D2PAK-7L | TO-247-3L | TO-247-4L | TO-247-4L Notch | TSPAK-DBC | TSPAK-LF |
|---|---|---|---|---|---|---|---|---|
| | |  |  |  |  |  |  |  |
| 16mΩ | Industrial | PCO120N16M2 | | PCW120N16M2 | PCZ120N16M2 | PCZN120N16M2 | | |
| | Automotive | PCO120N16M2A | | | | PCZN120N16M2A | | |
| 21mΩ | Industrial | PCO120N21M2 | | | PCZ120N21M2 | PCZN120N21M2 | | |
| | Automotive | PCO120N21M2A | PCBF120N21M2A | | | PCZN120N21M2A | PCRZ120N21M2A | PCR120N21M2A |
| 31mΩ | Industrial | PCO120N31M2 | | | PCZ120N31M2 | PCZN120N31M2 | | |
| | Automotive | PCO120N31M2A | PCBF120N31M2A | | | PCZN120N31M2A | | |
| 40mΩ | Industrial | PCO120N40M2 | | PCW120N40M2 | PCZ120N40M2 | PCZN120N40M2 | PCRZ120N40M2 | PCRZ120N40M2 |
| | Automotive | PCO120N40M2A | PCBF120N40M2A | | | PCZN120N40M2A | PCRZ120N40M2A | PCR120N40M2A |
| 60mΩ | Industrial | PCO120N60M2 | | | PCZ120N60M2 | PCZN120N60M2 | | |
| | Automotive | PCO120N60M2A | PCBF120N60M2A | | | | PCRZ120N60M2A | PCR120N60M2A |
| 80mΩ | Industrial | PCO120N80M2 | | | PCZ120N80M2 | PCZN120N80M2 | | |
| | Automotive | PCO120N80M2A | PCBF120N80M2A | | | | | |

For more product information, please visit https://www.powermastersemi.com

## 6.2. Nomenclature

Device part number contains a lot of information such as technology, package, voltage rating and generation, etc. Fig. 10 shows Power Master Semiconductor's $e$SiC MOSFET nomenclature

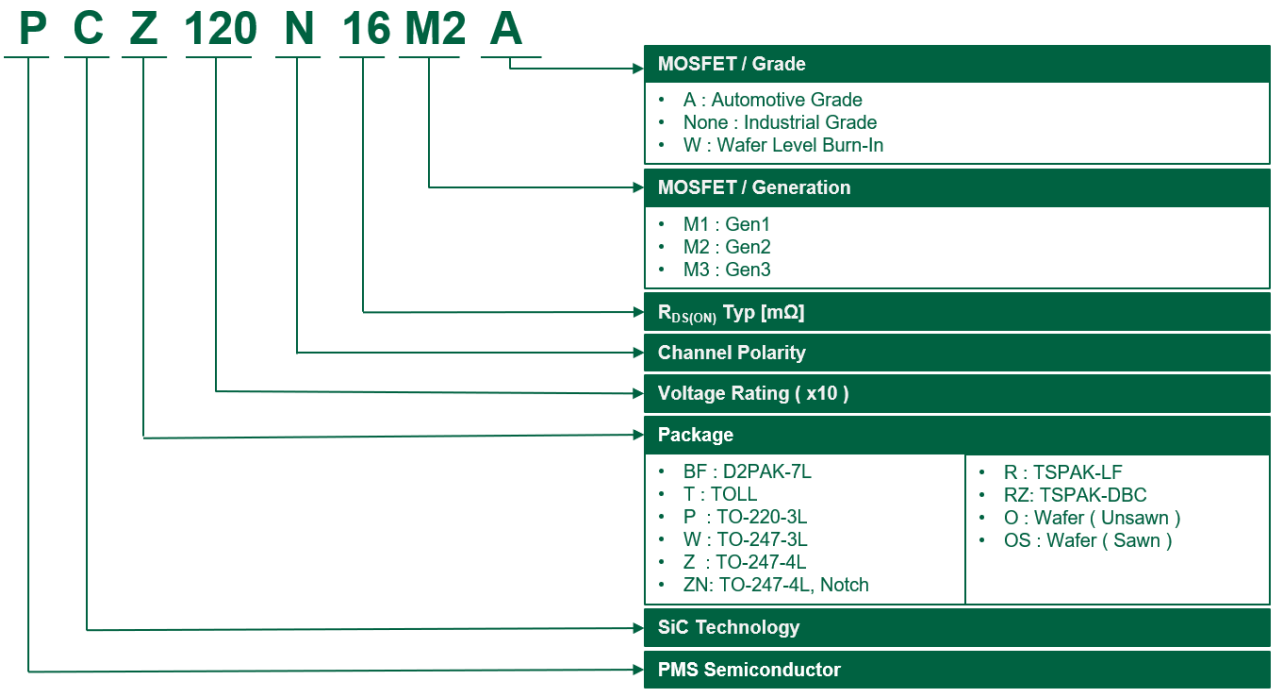


**Figure 10.** $e$SiC MOSFET nomenclature scheme

# 7. Document Revision History

**Major changes since the last version**

| Date | Description of change |
|---|---|
| 22-October-2025 | First Release |

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